



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/955,310 | 09/19/2001 | Sung-min Yim | SEC.813 | 8171 |

7590 09/04/2003
VOLENTINE FRANCO, P.L.L.C.
SUITE 150
12200 SUNRISE VALLEY DRIVE
RESTON, VA 20191

EXAMINER

CHAN, EMILY Y

ADT INIT DATED NUMBER

2829

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|----------------------------|--|
| Office Action Summary | Application No. 09/955,310 | Applicant(s) YIM ET AL. | |
| | Examiner emily y chan | Art Unit 2829 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: |

DETAILED ACTION

Claims 1-19 are presented for examination

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the **“any output driver of the semiconductor device”** recited in claims 1,9,15 and 18-19 **“an address pin of the semiconductor device”** recited in claims 2 and 16; **“a pad of a data input/output pin”** recited in claim 4; and **“a second pad that is connected to a data input/output pin”** recited in claims 18-19 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. For example, (1) the structural connection for the **“any output driver of the semiconductor device”**; (2) the structural connection for **“pad of a data input/output pin”**; and (3) the structural connection for the **“second pad that is connected to a data input/output pin”** are not shown in drawings or described in

Art Unit: 2829

detail in the specification as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 4, 9, and 18-19, the location of the semiconductor device is unclear. According to Fig 5 of the specification, the semiconductor device or the electrical elements (TNV, TNI, TPV, TPI and RS) **are located inside or are part** of the electrical characteristic measurer (50); however, the way it claims such as "an electrical characteristic measurer **that is connected** to the electrical element and a pad the semiconductor device" seems that the electrical elements (TNV, TNI, TPV, TPI and RS) **are located outside** of the electrical characteristic measurer (50). The examiner assumes that semiconductor device or the electrical elements are outside of the electrical characteristic measurer.

In claims 1, 9, and 15, and 18-19, the recitation "the pad **is not connected** to any output drive of the semiconductor device" is unclear since it is unclear where the "output drive" is and what the "output drive" stands for are not explained. The examiner assumes that the "output drive" is output connection for the semiconductor device according to page 9 lines 0031-0032 of specification.

In claim 4, since there are two "pad" recited, it is unclear whether the "pad" of semiconductor device is the same "pad" of the data input/output pin. The examiner

Art Unit: 2829

assumes that the "pad" of semiconductor device is the same "pad" of the data input/output pin.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1,3 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454) and further in view of Roberts et al ('661).

5. With respect to **claim 1**, Stambbaugh et al ('454) expressly teach a semiconductor device test circuits for determining fabrication parameters or measuring electrical characteristic of an electrical element within a packaged semiconductor device as claimed, comprising:

An electrical characteristic measurer (See Figs 3,6-9) (CMOS test circuits 40, 80; NMOS test circuit 94; PMOS test circuit 106 and resistive element test circuit 114) is connected to the electrical element (24 or 82) and a pad (28) of the semiconductor device. The electrical characteristic measurer is driven in response to a control signal (Fig. 5, 78) (See Col. 7, lines 60-61) to output to the pad (28) a value that is indicative of the electrical characteristic of an electrical element. The control signal (78) is activated in an electrical characteristic measuring mode or test mode after the semiconductor device is packaged (See Col. 8, lines 4-9).

Stambbaugh et al ('454) do not specify that their pad (28) **is not connected** to any output driver of the semiconductor device; however, It would have been obvious to one of ordinary skill in the art to understand that Stambbaugh et al ('454) 's pad (28) is **not connected** to any output driver of the semiconductor device since it is unknown what the "output driver" stands for (See 35 USC 112 rejection above).

6. With respect to **claims 3 and 5-8**, Stambbaugh et al ('454) teach that their electrical element is a transistor and selected from a group including an NMOS transistor (see Fig 7, element 96), a PMOS Transistor (see Fig 8 element 108) and a resistor (see Fig 9, element 118). Stambbaugh et al ('454) also teach that the value is Indicative of one a threshold voltage and a saturation current of NMOS transistor, one of the threshold voltage and saturation current of the PMOS transistor and a resistance of the resistor (see col. 5, lines 65-66 and col. 10, lines 67-68).

7. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454) as applied to claim 1 above, and further in view of Roberts et al ('661).

Stambbaugh et al ('454) do not teach that their control signal generator or test mode circuit (76) receives **at least one bit of an address pin** of the semiconductor device and that generates the control signal responsive thereto.

Roberts et al ('661) disclose an apparatus for providing external access to internal integrated circuit test circuits and expressly teach that a control signal generator (See Fig 11 element 122 below) receives **at least one bit of an address pin** (A0, n A1)

Art Unit: 2829

of the semiconductor device and generate the control signal (TEST1, TEST2, TEST3, TEST4) responsive thereto.

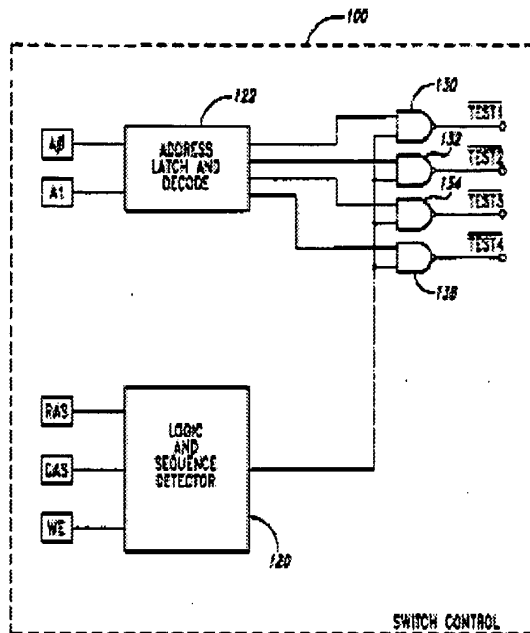


Fig. 11

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to have substituted the Stambbaugh et al ('454) 's control signal generator or test mode circuit by Roberts et al ('661)'s test signal generator 122 for generating test signals in responsive to a received address signal because both references are directed to test signal generation for measuring or testing electrical elements for packaged semiconductor device, and Stambbaugh et al ('454) 's and Roberts et al ('661)' s test signal generating circuit are functional equivalents as

Art Unit: 2829

suggested by Roberts et al ('661) (see col. 6, lines 35-36, and col. 7, lines 49-51).

Therefore, the substitution of functional equivalents in Stambbaugh et al ('454) would lead to the expected success.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454) in view of Roohparvar ('961).

Stambbaugh et al ('454) expressly teach a semiconductor device test circuits for determining fabrication parameters or measuring electrical characteristic of an electrical element within a packaged semiconductor device as claimed, comprising:

an electrical characteristic measurer (See Figs 3,6-9) (CMOS test circuits 40, 80; NMOS test circuit 94; PMOS test circuit 106 and resistive element test circuit 114) is connected to the electrical element (24,82, and 96 for Figs 3, 6 and 7) and a pad (28) of the semiconductor device. The electrical characteristic measurer is driven in response to a control signal (Fig. 5, 78)(See Col. 7, lines 60-61) to output to the pad (28) a value that is indicative of the electrical characteristic of an electrical element. The control signal (78) is activated in an electrical characteristic measuring mode or test mode after the semiconductor device is packaged (See Col. 8, lines 4-9).

Moreover, Stambbaugh et al ('454) particularly teach that electrical characteristic measurer (See Fig 7) includes an NMOS transistor (98), having a drain and source, one of the drain and the source being connected to the pad (28), and the other of the drain and the source being connected to a terminal of the electrical element (96).

Stambbaugh et al ('454) do not show that their one of same size NMOS transistor 102 is connected to a pad of a data input/output pin.

Roohparvar ('961) disclose a method for testing an integrated memory chip (see Fig. 1) and specifically teach an NMOS transistor (M1) which is connected to a pad of a data input/output pin (30) (See Col. 4, lines 22-26).

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the teaching of Roohparvar ('961) 's NMOS transistor connected to I/O (30) into Stambbaugh et al ('454) 's electrical characteristic measurer for the purpose of allowing match between input data through the I/O pin with internal test data and thus easily and quickly identify an electrical element or a memory cell having fault as disclosed by Roohparvar ('961) (See Col. 13, lines 27-30).

9. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454) in view of Roberts et al ('661).

With respect to claim 9, Stambbaugh et al ('454) expressly teach a semiconductor device test circuits for determining fabrication parameters or measuring electrical characteristic of an electrical element within a packaged semiconductor device as claimed, comprising:

an control signal generator (Fig. 5, 76) coupled to receive signals (70,72, 74) of the semiconductor device and generates a control signal (78);

an electrical characteristic measurer (See Figs 3,6-9) (CMOS test circuits 40, 80; NMOS test circuit 94; PMOS test circuit 106 and resistive element test circuit 114), to which the electrical element (elements 24 and 82 for Figs 3 and 6) is connected, that is driven responsive to the control signal (78) to output to a first pad (28) of the

Art Unit: 2829

semiconductor device a value indicative of the electrical characteristic of an electrical element.

Stambbaugh et al ('454) do not specify that their first pad (28) **is not connected** to any output driver of the semiconductor device; however, it would have been obvious to one of ordinary skill in the art to understand that Stambbaugh et al ('454) 's pad (28) is **not connected** to any output driver of the semiconductor device since it is unknown what the "output driver" stands for (See 35 USC 112 rejection above).

Stambbaugh et al ('454) do not teach that their control signal generator or test mode circuit (76) receives an address signal of the semiconductor device and that generates the control signal.

Roberts et al ('661) disclose an apparatus for providing external access to internal integrated circuit test circuits and expressly teach that a control signal generator (See Fig 11 element 122 below) receives **at least one bit of an address pin** (A0, A1) of the semiconductor device and generates the control signal (TEST1, TEST2, TEST3, TEST4) responsive thereto.

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to have substituted the Stambbaugh et al ('454) 's control signal generator or test mode circuit by Roberts et al ('661)'s test signal generator 122 for generating test signals in responsive to a received address signal because both references are directed to test signal generation for measuring or testing electrical elements for packaged semiconductor device, and Stambbaugh et al ('454) 's and Roberts et al ('661)' s test signal generating circuit are functional equivalents as

Art Unit: 2829

suggested by Roberts et al ('661) (see col. 6, lines 35-36, and col. 7, lines 49-51).

Therefore, the substitution of functional equivalents in Stambbaugh et al ('454) would lead to the expected success.

10. With respect to **claims 10**, Stambbaugh et al ('454) teach that their electrical element is one of a transistor (24) and a resistor (108), their electrical characteristic measurer comprising at least one transistor characteristic measuring unit (See Figs 3,6-8) (CMOS test circuits 40, 80; NMOS test circuit 94; PMOS test circuit 106), and a resistor characteristic measuring unit (See Fig 9) (resistive element test circuit 114), as selectable by the control signal.

11. With respect to **claims 11**, Stambbaugh et al ('454) teach that their electrical characteristics of the transistor are one of a threshold voltage and saturation current (see col. 5, lines 65-66) of NMOS transistor, one of the threshold voltage and saturation current of the PMOS transistor and a resistance of the resistor and.

12. With respect to **claims 12**, Stambbaugh et al ('454) teach that their electrical characteristic of the resistor is a resistance (See Col. 10, lines 67-68).

13. With respect to **claims 13**, Roberts et al ('661)'s address signal only has two bits (A0, A1) of the address signal.

13. With respect to **claims 14**, Stambbaugh et al ('454) teach that their control signal (78) is generated during electrical characteristic measuring mode, after the semiconductor device is packaged. (See Col. 1, lines 62-65).

14. Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454).

Art Unit: 2829

With respect to claim 15, Stambbaugh et al ('454) teaches a method for determining fabrication parameters or measuring electrical characteristic of an electrical element within a semiconductor device in a packaged state, comprising:

(1), connecting the electrical element (NCOMS transistor) of the semiconductor device to an electrical characteristic measurer (See Figs 3,6-9) (CMOS test circuits 40, 80; NMOS test circuit 94; PMOS test circuit 106 and resistive element test circuit 114), after the semiconductor device is packaged;

(2), controlling the semiconductor device to enter a predetermined electrical characteristic measuring mode (Fig 5, test mode detect circuit 76),

(3), generating a control signal (test signal)

(4) driving the electrical characteristic measurer responsive to the control signal (Fig. 5, 78) to output a value indicative of the electrical characteristic of an electrical element to a first pad (28) of the semiconductor device.

Stambbaugh et al ('454) do not specify that their first pad (28) of the semiconductor device **is not connected** to any output driver of the semiconductor device; however, It would have been obvious to one of ordinary skill in the art to understand that Stambbaugh et al ('454) 's pad (28) **is not connected** to any output driver of the semiconductor device since it is unknown what the "output driver" stands for (See 35 USC 112 rejection above).

15. With respect **claim 17**, Stambbaugh et al ('454) particularly teach that their electrical element is selected from a group including an NMOS transistor (see Fig 7, element 96), a PMOS Transistor (see Fig 8 element 108) and a resistor (see Fig 9,

Art Unit: 2829

element 118). Stambbaugh et al ('454) also teach that the value outputted during the driving is indicative of one a threshold voltage and a saturation current of NMOS transistor, one of the threshold voltage and saturation current of the PMOS transistor and a resistance of the resistor (see col. 5, lines 65-66 and col. 10, lines 67-68).

16. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454) as applied to **claim 15** above, and further in view of Roberts et al ('661).

Stambbaugh et al ('454) do not teach that their control signal generator or test mode circuit (76) receives address signal provided to an address pin of the semiconductor device.

Roberts et al ('661) disclose an apparatus for providing external access to internal integrated circuit test circuits and expressly teach that a control signal generator (See Fig 11 element 122 below) receiving an address signal provided to an address pin (A0, A1) of the semiconductor device and entering into a specific sub mode of the electrical characteristic measuring mode responsive to a value of at least one bit of the address signal.

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the teaching of Roberts et al ('661)'s address signals into Stambbaugh et al ('454) 's control signal generator or test mode circuit for the purpose of generating test signals in responsive to a received address signal because both references are directed to test signal generation for measuring or testing electrical elements for packaged semiconductor device, and Stambbaugh et al ('454) 's and

Art Unit: 2829

Roberts et al ('661)' s test signal generating circuit are functional equivalents as suggested by Roberts et al ('661) (see col. 6, lines 35-36, and col. 7, lines 49-51).

17. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454) as applied to **claims 9 and 15 respectively** above, and further in view of Roohparvar ('961).

Stambbaugh et al ('454) expressly teach that their electrical characteristic measurer (See Fig 7, 94) includes an NMOS transistor (98) having a drain and source, one of the drain and source being connected to the first pad (28), and the other of the drain and the source being connected to a the first pad (28) and the other of the drain and the source being connected to a terminal of the electrical element (96).

Stambbaugh et al ('454) do not show that their one of same size NMOS transistor 102 is connected to a data input/output pin.

Roohparvar ('961) disclose a method for testing an integrated memory chip (see Fig. 1) and specifically teach an NMOS transistor (M1) which is connected to a pad of a data input/output pin (30) (See Col. 4, lines 22-26).

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the teaching of Roohparvar ('961) 's NMOS transistor connected to I/O (30) into Stambbaugh et al ('454) 's electrical characteristic measurer for the purpose of allowing match between input data through the I/O pin with internal test data and thus easily and quickly identify an electrical element or a memory cell having fault as disclosed by Roohparvar ('961) (See Col. 13, lines 27-30).

Art Unit: 2829

18. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

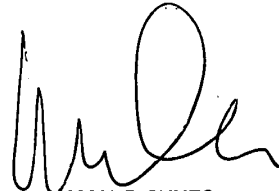
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily y Chan whose telephone number is 7033056123. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo Kammie can be reached on 7033081233. The fax phone numbers for the organization where this application or proceeding is assigned are 7033085841 for regular communications and 7033085841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7022056123.

ec
August 20, 2003



KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800